WHAT IS CLAIMED IS:

1. A digital processing system for decoding convolutional encoded data comprising:

circuit means for performing branch metrics calculations;

circuit means for performing path metrics calculations;

survivor storage for retaining survivor bits indicating a preferred path through a tree;

a pipeline register for receiving a word of survivor bits from said survivor storage;

a trace-back circuit for selecting a tree path and for determining a next address in said survivor storage; and

means for compensating for the delay introduced by said pipeline register.

2. The digital processing system of Claim 1 wherein said compensating means comprises storage of said survivor bits in a non-ordinal sequence.

3. The digital processing system of Claim 1 wherein said compensating means comprises storage of said survivor bits based on an optimized subsection of said tree.

4. The digital processing system of Claim 1 wherein said compensating means comprises storage of said survivor bits based on a final state distribution.

5. The digital processing system of Claim 1 wherein the selection of a survivor bit for addressing a word from said survivor storage for transfer to said pipeline register.

6. The digital processing system of Claim 1 wherein said pipeline comprises a single stage and said memory is organized into an even word and an odd word.

7. The digital processing system of Claim 6 wherein said even word corresponds to the following states: 0, 32, 16, 48, 8, 40, 24, 56, 4, 36, 20, 52, 12, 44, 28, 60, 2, 34, 18, 50, 10, 42, 26, 58, 6, 38, 22, 54, 14, 46, 30 and 62.

8. The digital processing system of Claim 6 wherein said odd word corresponds to the following states: 1, 33, 17, 49, 9, 41, 25, 57, 5, 37, 21, 53, 13, 45, 29, 61, 3, 35, 19, 51, 11, 43, 27, 59, 7, 39, 23, 55, 15, 47, 31 and 63.

9. The digital processing system of Claim 1 wherein said pipeline comprises a single stage and said memory is organized into two 32 bit memory words.

10. The digital processing system of Claim 1 wherein said pipeline comprises a single stage and said memory is organized into a first word for storing the first 16 bits and bits 32-47 and a second word for storing bits 16-31 and bits 48-63.

11. A method for obtaining the maximum likelihood sequence estimate of bits in a data stream from a convolutionally encoded received data stream comprising the steps of:

Performing the following steps for each received bit in said encoded received data stream:

a. Determining a trace-back length;

b. Obtaining a Trellis diagram of the convolutional encoder that generated said encoded received data stream;

c. Obtaining the number of the states in a Trellis obtained from said encoder;

d. For each bit in said received data stream, perform a plurality of forward butterfly computations to determine survivor path bits;

e. For each butterfly computation, storing the resulting survivor path bits for each state in a memory;

f. For each butterfly computation, updating path metrics for a pair of states and generating a pair of survivor bits; and

g. Repeating steps a-f for each bit until all bits in the encoded received data stream have been recorded;

Selecting a trace-back window;

Sequentially decrementing by 2 32-bit word steps to access a trace-back memory;

Extracting a trace bit from said accessed memory word to identify the path to a previous state in the survivor path;

Using said trace bit to perform a look-ahead function to determine a computed address of a future survivor word;

Determining whether said future survivor word is an even or odd state;

Determining a decoded bit from said computed address; and

Outputting an unencoded data stream corresponding to said encoded received data stream.

12. The method of Claim 11 wherein the information stored in said trace-back memory is partitioned.

13. The method of Claim 12 wherein the information stored in said trace-back memory is partitioned into an even partition and an odd partition.

14. The method of Claim 13 wherein said memory partitions correspond to a code tree.

15. The method of Claim 13 wherein the constraint length (k) of said encoder is an odd integer.

16. The method of Claim 12 wherein the parameters of said encoder are: rate (r) where r = ½; constraint length (k) where k = 7; and generator polynomials $g_0 = 133|_8$ and $g_1 = 171|_8$.

17. The method of Claim 12 wherein the said encoders has a rate (r) where r = ½ and a constraint length (k), where k = 9.

18. A system to implement the method of Claim 11.

19. A computer to implement the method of Claim 11.

20. A computer-readable medium having instructions for assisting in the implementation of the method of Claim 11.

21. A method for implementing a Viterbi decoder comprising the steps of:

Receiving convolutionally encoded data;

Generating a tree for said encoded data;

Calculating branch metrics;

Calculating path metrics to determine survivor bits indicating a preferred path through a tree;

Retaining said survivor bits in a memory;

Selectively accessing words in said memory using a look-ahead pipeline;

a trace-back circuit for selecting a tree path and for determining a next address in said survivor storage; and

means for compensating for the delay introduced by said pipeline register.

22. The method of Claim 21 wherein the information stored in said trace-back memory is partitioned.

23. The method of Claim 21 wherein the information stored in said trace-back memory is partitioned into an even partition and an odd partition.

24. The method of Claim 23 wherein said memory partitions correspond to a tree.

25. The method of Claim 22 wherein the parameters of said encoder are: rate (r) where r = ½; constraint length (k) where k = 7; and generator polynomials $g_0 = 133|_8$ and $g_1 = 171|_8$.

26. The method of Claim 22 wherein the said encoders has a rate (r) where r = ½ and a constraint length (k) where k = 9.

27. A system to implement the method of Claim 21.

28. A computer to implement the method of Claim 21.

29. A computer-readable medium having instructions for assisting in the implementation of the method of Claim 21.

30. A method for implementing a Viterbi decoder, having a pipeline register, that maintains data throughput and integrity comprising the steps of:

Organizing a memory for storing survivor bits to account for pipeline delay where said organization is based upon the properties of the code tree;

Receiving convolutionally encoded data;

Decoding said received convolutionally encoded data; and

Outputting data corresponding to said received convolutionally encoded data.

31. The method of Claim 30 wherein said memory is organized so that the storage of survivor bits is in a non-ordinal sequence.

32. The method of Claim 30 wherein said memory is organized so that the storage of said survivor bits is based on an optimized subsection of a code tree.

33. The method of Claim 32 wherein said code tree is defined by the parameters of said encoder.

34. The method of Claim 30 further comprising the step of selecting of a survivor bit for addressing a word from said memory for transfer to said pipeline register.

35. The method of Claim 30 wherein said memory is organized into an even word and an odd word.

36. The method of Claim 30 wherein said even word corresponds to the following states: 0, 32, 16, 48, 8, 40, 24, 56, 4, 36, 20, 52, 12, 44, 28, 60, 2, 34, 18, 50, 10, 42, 26, 58, 6, 38, 22, 54, 14, 46, 30 and 62.

37. The method of Claim 30 wherein said odd word corresponds to the following states: 1, 33, 17, 49, 9, 41, 25, 57, 5, 37, 21, 53, 13, 45, 29, 61, 3, 35, 19, 51, 11, 43, 27, 59, 7, 39, 23, 55, 15, 47, 31 and 63.

38. The method of Claim 37 wherein said pipeline comprises a single stage and said memory is organized into two 32-bit memory words.

39. The method of Claim 30 wherein said pipeline comprises a single stage and said memory is organized into a first word for storing the first 16 bits and bits 32-47 and a second word for storing bits 16-31 and bits 48-63.

40. A system to implement the method of Claim 30.

41. A computer to implement the method of Claim 30.

42. A computer-readable medium having instructions for assisting in the implementation of the method of Claim 30.